CLAIMS

What is claimed is:

1. A nested transimpedance amplifier (TIA) circuit, comprising:

a zero-order TIA having an input and an output;

a first operational amplifier (opamp) having an input that communicates with said output of said zero-order TIA and an output; and

a first feedback resistance having one end that communicates with said input of said zero-order TIA and an opposite end that communicates with said output of said first opamp.

2. The nested TIA circuit of claim 1 further comprising a capacitor having one end that communicates with said input of said zero-order TIA.

3. The nested TIA circuit of claim 2 wherein said zero order TIA includes a second opamp having an input and an output and a third opamp having an input that communicates with said output of said second opamp and an output.

4. The nested TIA circuit of claim 3 wherein said zero order TIA includes a second feedback resistance having one end that communicates with said input of said third opamp and an opposite end that communicates with said output of said third opamp.

5. The nested TIA circuit of claim 4 further comprising a fourth opamp having an input and an output that communicates with said input of said second opamp.

6. The nested TIA circuit of claim 5 further comprising a fifth opamp having an input that communicates with said output of said first opamp and an output.

7. The nested TIA circuit of claim 6 further comprising a third feedback resistance having one end that communicates with said input of said fourth opamp and an opposite end that communicates with said output of said fifth opamp.

8. The nested TIA circuit of claim 1 further comprising at least one higher order circuit that is connected to said nested TIA circuit and includes an n^{th} feedback resistance, an n^{th} opamp, and an $(n+1)^{th}$ opamp.

9. The nested TIA circuit of claim 1 wherein said first feedback resistance is one of a standard fixed-value resistor, a nonlinear variable resistor and a metal-oxide-semiconductor (MOS) resistor.

10. The nested TIA circuit of claim 1 wherein said first opamp includes one of bipolar junction transistors and metal-oxide-semiconductor transistors.

11. The nested TIA circuit of claim 1 wherein said first opamp includes metal-oxide-semiconductor transistors and a bandwidth of said nested TIA circuit is greater than 10% of a threshold frequency.

12. The nested TIA circuit of claim 1 wherein said nested TIA circuit is implemented in an optical sensor.

13. The nested TIA circuit of claim 1 wherein said nested TIA circuit is implemented in a preamplifier of a hard disk drive.

14. A nested differential mode TIA circuit, comprising:

a zero-order differential mode TIA having first and second inputs and first and second outputs;

a first differential mode opamp having first and second inputs that communicate with said first and second outputs of said zero-order differential mode TIA and first and second outputs;

a first feedback resistance having one end that communicates with said first input of said zero-order differential mode TIA and an opposite end that communicates with said first output of said zero-order differential mode TIA; and

a second feedback resistance having one end that communicates with said second input of said zero-order differential mode TIA and an opposite end that communicates with said second output of said zero-order differential mode TIA.

15. The nested differential mode TIA circuit of claim 14 wherein said zero order differential mode TIA includes a second differential mode opamp having first and second inputs and first and second outputs.

16. The nested differential mode TIA circuit of claim 15 wherein said zero order TIA includes a third differential mode opamp having first and second inputs that communicates with said first and second outputs of said second differential mode opamp and first and second outputs.

17. The nested differential mode TIA circuit of claim 16 wherein said zero order TIA includes a third feedback resistance having one end that communicates with said first input of said third differential mode opamp and an opposite end that communicates with said first output of said third differential mode opamp.

18. The nested TIA circuit of claim 17 wherein said zero order TIA includes a fourth feedback resistance having one end that communicates with said second input of said third differential mode opamp and an opposite end that communicates with said second output of said third differential mode opamp.

19. The nested TIA circuit of claim 14 further comprising at least one higher order circuit that is connected to said nested TIA circuit and includes an n^{th} feedback resistance, an $(n+1)^{th}$ feedback resistance, and an n^{th} differential mode opamp.

20. The nested TIA circuit of claim 14 wherein said first feedback resistance is one of a standard fixed-value resistor, a nonlinear variable resistor and a metal-oxide-semiconductor (MOS) resistor.

21. The nested TIA circuit of claim 14 wherein said first opamp includes one of bipolar junction transistors and metal-oxide-semiconductor transistors.